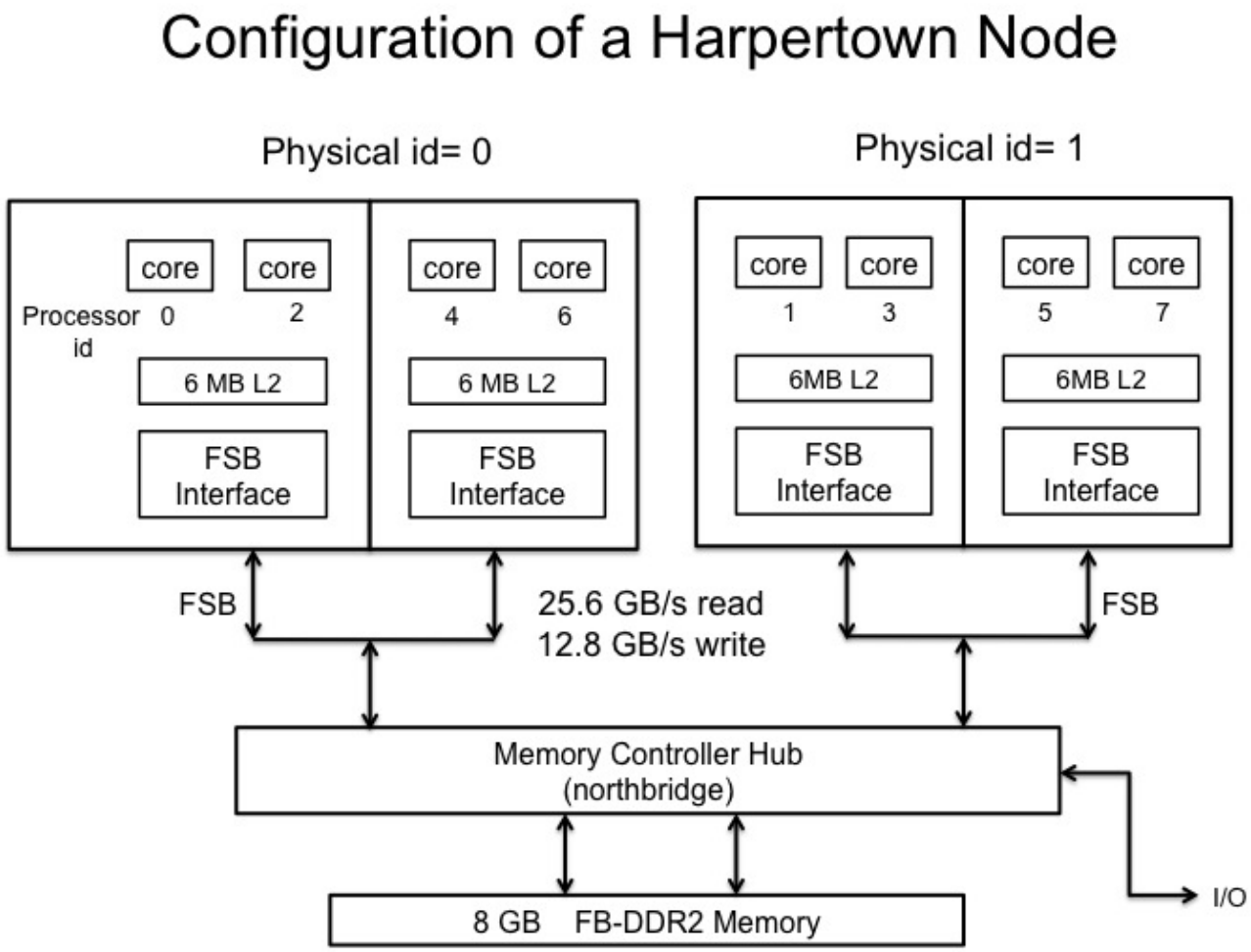
Harpertown Processors

Category: Pleiades

DRAFT

This article is being reviewed for completeness and technical accuracy.

Configuration of a Harpertown node:



Core Labeling:

The core labeling as shown in this diagram is obtained from the command *cat /proc/cpuinfo*. Note that in the first socket (i.e., phyiscal id=0), the four cores are labeled 0, 2, 4, and 6,

and are not contiguous. Similarly, in the second socket (physical id=1), they are labeled as 1, 3, 5, and 7. In addition, each core pair (0,2), (4,6), (1,3) and (5,7) shares a 6MB L2 cache.

For performance consideration, care must be taken if one tries to use tools such as *dplace* to pin processes to specific processors. Be aware of the non-contiguous nature of the labeling and the sharing of L2 cache per core pair. Also, when using the SGI MPT library, the environment variable **MPI_DSM_DISTRIBUTE** has been set to *off* for the Harpertown nodes since setting MPI_DSM_DISTRIBUTE to *on* causes the processes to be pinned to processors in a contiguous order. For example, MPI ranks 0-7 are pinned to processors 0-7, respectively. This results in bad performances for most applications.

SSE4 Instruction Set:

Intel's Streaming SIMD Extensions 4.1 (SSE4.1) instruction set is included in the Harpertown processors.

Since the instruction set is upward compatible, an application which is compiled with -xSSE4.1 (with Intel version 11 compiler) can run on either Harpertown or Nehalem-EP or Westmere processors. An application which is compiled with -xSSE4.2 can run ONLY on Nehalem-EP or Westmere processors.

If you wish to have a single executable that will run on any of the three Pleiades processor types with suitable optimization to be determined at run time, you can compile your application with -O3 -ipo -axSSE4.2,xSSE4.1

Hyperthreading:

Not available.

Turbo Boost:

Not available.

Front-Side Bus

The Harpertown (Quad-Core Intel Xeon Processor E5472) processors at NAS use 1600 MHz Front-Side Bus (FSB). The processor transfers data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a double-clocked or a 2X address bus. In addition, the Request Phase completes in one clock cycle. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 12.8 GBytes per second. The FSB is also used to deliver interrupts.

Article ID: 78
Last updated: 24 May, 2011
Computing at NAS -> Computing Hardware -> Pleiades -> Harpertown Processors
http://www.nas.nasa.gov/hecc/support/kb/entry/78/?ajax=1